REMARKS

This is a full and timely response to the non-final Official Action dated January 7, 2010 (the "Office Action" or "Action"). Reconsideration of the application in light of the above amendments and the following remarks is respectfully requested.

Claim Status:

Under the imposition of a previous Restriction Requirement, claims 2, 12-15, 17-25, 36, 37, 42-46, and 50-54 have been withdrawn from consideration and are marked accordingly above. Claims 7, 34, and 35 were previously cancelled without prejudice or disclaimer.

Claims 5, 27, 39, 48-49, and 56-57 have been amended. The present paper proposes no other changes to the claims.

Objection to Claims:

Claims 27-29, 31-32, 39-41, 48-49, and 56-57 were objected to under 37 C.F.R. § 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim. According to the Examiner, the "memory array, the substrate, the integrated circuit [sic] do not further limit the structure claimed in the respective independent claims. Applicant strongly disagrees.

With regard to independent claim 26, claim 27 recites "[a] memory array comprising a multiplicity of the memory cells of claim 26," claim 28 recites "[a] memory array carrying electronics comprising the memory array of claim 27," and claim 29 recites "[a]n integrated circuit comprising the memory array of claim 27."

With regard to independent claim 30, claim 31 recites "[a] substrate carrying electronics comprising the multilayer memory of claim 30," and claim 32 recites "[a]n integrated circuit comprising the multilayer memory of claim 30."

With regard to independent claim 38, claim 39 recites "[a] memory array comprising a multiplicity of the memory cells of claim 26," claim 40 recites "[a] substrate carrying electronics comprising the memory cells of claim 39," and claim 41 recites "[a]n integrated circuit comprising the memory array of claim 39."

With regard to independent claim 47, claim 48 recites "[a] substrate carrying electronics comprising the multilayer memory of claim 47," and claim 49 recites "[a]n integrated circuit comprising the multilayer memory of claim 47."

Finally, with regard to independent claim 55, claim 56 recites "[a] substrate carrying electronics comprising the multilayer memory of claim 55," and claim 57 recites "[a]n integrated circuit comprising the multilayer memory of claim 55."

Applicant respectfully notes that each of claims 26, 38, 47, and 55 is a product-by process type claim. The M.P.E.P. very plainly and explicitly states that "although 37 C.F.R. § 1.75(c) requires the dependent claim to further limit a preceding claim, ***this rule does not apply to product-by-process claims***." Because claims 27-29, 39-41, 48-49, and 56-57 are all dependent product-by-process claims, the Examiner's position that claims 27-29, 39-41, 48-49, and 56-57 do not comply with 37 C.F.R. § 1.75(c) is moot, as 37 C.F.R. § 1.75(c) does not apply to claims 27-29, 39-41, 48-49, and 56-57. Thus, for at least this reason alone, the objection to claims 27-29, 39-41, 48-49, and 56-57 under 37 C.F.R § 1.75(c) should be withdrawn.

Furthermore, if a dependent claim fails to limit the structure of its respective independent claim, then by definition any structure that infringes the independent claim must

necessarily infringe the dependent claim. This is not the case with claims 27-29, 31-32, 39-41, 48-49, and 56-57. A structure that infringes one of independent claims 26, 30, 38, 47, and 55 would not necessarily infringe any of claims 27-29, 31-32, 39-41, 48-49, and 56-57, respectively, because each of claims 27-29, 31-32, 39-41, 48-49, and 56-57 recites additional structures beyond what is recited in its corresponding independent claim. Therefore, the Examiner has incorrectly asserted that claims 27-29, 31-32, 39-41, 48-49, and 56-57 fail to further limit the structure claimed in the respective independent claims, and the present objection to these claims should be withdrawn.

35 U.S.C. § 112, second paragraph:

The final Office Action rejects claims 4, 5, and 27 as being indefinite under 35 U.S.C. § 112, second paragraph.

Claim 4:

Claim 4 recites "[t]he memory array of claim 1, wherein the silicon-rich insulator of each memory cell is electrically isolated from the silicon-rich insulators of all other memory cells." According to the Action, it "is unclear as to how one element (the silicon-rich insulator) in one memory array can be electrically isolated from plurality [sic] of elements (the silicon-rich insulators) of all other memory cells, since all the memory cells in one memory array are electrically connected to each other." (Action, pp. 2-3). Applicant respectfully disagrees.

The Examiner is incorrectly assuming that where all memory cells are electrically connected to each other, every single component of each memory cell must be electrically connected to ever single component of every other memory cell. This assumption is logically fallible. Consider the example of a group of batteries connected in parallel such that each positive terminal of each battery is connected to a common positive node, and each negative terminal of each battery is connected to a common negative node. Each of the batteries is "electrically connected to each other," but without a circuit between the common positive node and common negative node, it cannot be said that the positive node of each battery is electrically connected to the negative node of every other battery.

The same is true by analogy with regard to claim 4. Just because certain elements of each memory cell are connected to other memory cells does not imply or require that every element of every memory cell be connected to every element of every other memory cell. As such, the objection to claim 4 is based on incorrect logic, and cannot stand. Therefore, the rejection to claim 4 based on 35 U.S.C. § 112, second paragraph, must be withdrawn.

Claim 5:

With regard to claim 5, the Action argues that the previously claimed "tunnel junction layer" is unclear "as to the structural relationship between the tunnel junction layer and the memory array." (Action, p. 3). Applicant respectfully disagrees. However, in the interest of cooperation and the expedition of prosecution, claim 5 has been amended to address the issues raised by the Examiner. Consequently, the rejection of claim 5 based on 35 U.S.C. § 112, second paragraph, should be withdrawn.

Claim 27:

Regarding claim 27, the Action points out that the previously claimed limitation of "the memory cells," was unclear in light of the fact that claim 26 recites only one memory cell. In response, Applicant has amended claim 27 to address the issues raised by the Examiner. Consequently, the rejection of claim 27 based on 35 U.S.C. § 112, second paragraph may now be withdrawn.

Prior Art:

1. Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49, and 55-59 were rejected under 35 U.S.C. § 103(a) as being obvious over D.J. DiMaria et al., *Dense Alpha Particle-Immune Memory Device*, IBM Technical Disclosure Bulletin, Jun. 1980, at 381 ("DiMaria") in view of U.S. Patent No. 6,881,994 to Lee et al. ("Lee") and U.S. Patent No. 6,834,008 to Rinerson et al. ("Rinerson"). These same claims were rejected alternatively under § 103(a) as being obvious over Lee in view of DiMaria. For at least the following reasons, these rejections are respectfully traversed.

Claim 1:

Claim 1 recites:

> A memory array comprising:
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, *each storage element comprising a low-resistance filament disposed therein,* each control element including a tunnel junction and a silicon-rich insulator, *wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the*

row conductor and the column conductor, and wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.

(Emphasis added).

To begin, Applicant respectfully notes that "[t]he examiner bears the initial burden . . . of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). A *prima facie* case of obviousness made under 35 U.S.C. § 103(a) requires a showing that all of the subject matter in the claim at issue would be obvious to one having ordinary skill in the art based on the teachings of the cited prior art. *See* M.P.E.P. § 2143. The recent Office Action does not make a *prima facie* case of obviousness against claim 1 because it fails to provide sufficient evidence that the cited prior art would render all of the subject matter of claim 1 obvious to one having ordinary skill in the art at the time of the invention. *Id.*

DiMaria is a single-page reference directed to a "dense alpha particle-immune memory device." (DiMaria, p. 382). DiMaria teaches a two-terminal memory device including a contact layer, a first oxide tunnel layer, a floating polysilicon storage layer, a first injector layer, a second oxide tunnel layer, a second injector, and a second contact layer. Nevertheless, DiMaria fails to teach or suggest "a storage element comprising a low-resistance filament disposed therein" such that "the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 1).

Lee fails to remedy the shortcomings of DiMaria. The Examiner has already conceded on the record that Lee does "not teach a control element including a tunnel junction and a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected." (Final Office Action of Oct. 21, 2008, p. 4). As such, Applicant notes that Lee *cannot* teach or suggest a storage element having a low-

resistance filament disposed therein that "electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 1). Even if *arguendo* Lee did teach or suggest such a silicon-rich insulator, Applicant that Lee would still fail to teach the storage element recited in claim 1, since Lee fails to teach a "storage element comprising a low-resistance filament disposed therein" at all, irrespective of any electrical connections made by the filament. (Claim 1).

In this regard, the Action takes the position that

> [b]oth Dimaria et al. and Lee et al. teach a memory device comprising a 'write' operation, which enables data to be written. Since a filament is defined as a "single thread or a thin flexible threadlike object," then as [sic] least part of the "write" operation of prior art's device can be defined as being made by "a single thread or a thin flexible threadlike object," which is part of the material of the storage material. That is, the "write" operation is done by a "filament." Therefore, prior art's device comprises "each storage element comprising a low-resistance filament [i.e., a single thread or a thin flexible threadlike object which provides the write operation] disposed therein, wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor," as claimed.

(Action, p. 20).

Applicant respectfully disagrees. The Action asserts that a filament is part of the "storage material" of the prior art. (*Id.*). However, the Action has failed to cite to any portion of the prior art that teaches or suggests such a filament. According to the Supreme Court, the Examiner is required to provide an explicit analysis as to how the cited prior art teaches or suggests all the features of a claim. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007) (citing to *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). "To facilitate review, this [the Examiner's] analysis should be made explicit." *Id.* As demonstrated above, the Examiner has failed to meet this burden with regard to claim 1. Therefore, under the standard of *KSR*, no *prima facie* case of obviousness has been made as to claim 1. For at least this reason alone, the rejection of claim 1 should be reconsidered and withdrawn.

Moreover, Applicant notes that even if DiMaria and Lee did teach a "filament," both of these references fail to teach or suggest a "low-resistance filament disposed" in a "storage element" such that the filament "electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 1). This subject matter is simply outside the scope of DiMaria and Lee. By asserting otherwise, the Examiner is unfairly reading subject matter from the prior art that simply does not exist.

Rinerson fails to remedy the deficiencies of DiMaria and Lee in teaching or suggesting the subject matter of claim 1. Specifically, Rinerson also fails to teach or suggest a "storage element comprising a low-resistance filament disposed therein" or that "the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 1).

Applicant notes that the present rejection relies on an assertion of obviousness based on the combination of prior art elements according to known methods to yield predictable results. According to the M.P.E.P., "[t]o reject a claim based on this rationale, Office personnel must resolve the . . . factual inquiries" of *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1 (1966). M.P.E.P. § 2143.

Under the analysis required by *Graham*, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. *Graham*, 383 U.S. at 17-18. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR Int'l v. Teleflex Inc.*, 550 U.S. 398, 407 (2007). While it is true that attacking references individually is not sufficient to demonstrate nonobviousness, *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981), the scope and content of the prior art as a whole may only be

determined by a methodical examination of each prior art reference to determine what each reference teaches and does not teach. If such an examination reveals that *each* cited prior art reference fails to teach or suggest a particular claimed element, it follows that the scope and content of the cited prior art does not include that element.

Applying the *Graham* analysis to the present case, the scope and content of the prior art, as evidenced by DiMaria, Lee, and Rinerson, did not include the claimed subject matter, particularly "each storage element comprising a low-resistant filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 1).

The differences between the cited prior art and the indicated claims are significant because the low-resistance filament provides an improved way of writing data into a storage element such as a tunnel-junction oxide or a state-change layer. (Applicant's Specification, p. 8, lines 26-28). Thus, the claimed subject matter provides features and advantages not known or available in the cited prior art. Consequently, the cited prior art will not support a rejection of claim 1 under 35 U.S.C. § 103 and *Graham*. For at least these reasons, the rejection of claim 1 and its dependent claims based on DiMaria, Lee, and Rinerson, or alternatively based on Lee and DiMaria, should be reconsidered and withdrawn.

Claim 16:

Claim 16 recites:

> A memory array comprising:
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for

> controlling being coupled in series between a row conductor and a column conductor, *each means for storing data comprising a low-resistance filament disposed therein,* each means for controlling including a tunnel junction and a silicon-rich insulator, *wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor*, and wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.

(Emphasis added).

In contrast, the cited prior art does not render the memory array of claim 16 obvious. Specifically, as amply demonstrated above, DiMaria, Lee, and Rinerson fail to teach or suggest, collectively or separately, "each means for storing data comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 16).

Again, under the analysis required by *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966), to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by DiMaria, Lee, and Rinerson, did not include the claimed subject matter, particularly "each means for storing data comprising a low-resistant filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 16).

The differences between the cited prior art and the indicated claims are significant because the low-resistance filament provides an improved way of writing data into a storage

element such as a tunnel-junction oxide or a state-change layer. (Applicant's Specification, p. 8, lines 26-28). Thus, the claimed subject matter provides features and advantages not known or available in the cited prior art. Consequently, the cited prior art will not support a rejection of claim 16 under 35 U.S.C. § 103 and *Graham*. For at least these reasons, the rejection of claim 16 and its dependent claims based on DiMaria, Lee, and Rinerson, or alternatively based on Lee and DiMaria, should be reconsidered and withdrawn.

Claim 26:

Claim 26 recites:

> A memory cell made by a method comprising:
> a) providing a substrate,
> b) depositing and patterning a first conductive layer over the substrate,
> c) forming a storage layer over the patterned first conductive layer, *the storage layer comprising a low-resistance filament disposed therein*,
> d) forming a layer of silicon-rich insulator over the storage layer,
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and
> f) forming and patterning a second conductive layer over the tunnel-junction layer, whereby a memory-cell stack is formed, the stack having a storage layer, a silicon-rich insulator, and a tunnel-junction layer in series relationship between the first and second conductive layers, such that the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *wherein the low-resistance filament of the storage layer electrically interconnects the layer of silicon-rich insulator with the first conductive layer*, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.

(Emphasis added).

In contrast, the cited prior art does not render the memory cell of claim 26 obvious. Specifically, as amply demonstrated above, DiMaria, Lee, and Rinerson fail to teach or suggest, collectively or separately, "the storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the layer of silicon-rich insulator with the first conductive layer." (Claim 26).

Again, under the analysis required by *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966), to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by DiMaria, Lee, and Rinerson, did not include the claimed subject matter, particularly "the storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the layer of silicon-rich insulator with the first conductive layer." (Claim 26).

The differences between the cited prior art and the indicated claims are significant because the low-resistance filament provides an improved way of writing data into a storage element such as a tunnel-junction oxide or a state-change layer. (Applicant's Specification, p. 8, lines 26-28). Thus, the claimed subject matter provides features and advantages not known or available in the cited prior art. Consequently, the cited prior art will not support a rejection of claim 26 under 35 U.S.C. § 103 and *Graham*. For at least these reasons, the rejection of claim 26 and its dependent claims based on DiMaria, Lee, and Rinerson, or alternatively based on Lee and DiMaria, should be reconsidered and withdrawn.

Claim 38:

Claim 38 recites:

> A memory cell made by a method comprising:
> a) providing a substrate,
> b) depositing and patterning a first conductive layer over the substrate,
> c) forming a storage layer over the patterned first conductive layer, *said storage layer comprising a low-resistance filament disposed therein*,

d) forming a layer of silicon-rich insulator over the storage layer,
e) forming a tunnel-junction layer over the layer of silicon-rich insulator,
f) forming and patterning a second conductive layer over the tunnel-junction layer,
g) forming and patterning an interlayer dielectric over the storage layer,
h) forming an opening through the interlayer dielectric and extending to the storage layer, and
i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *and wherein the low-resistance filament of the storage layer electrically interconnects the silicon-rich insulator with the first conductive layer*, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.

(Emphasis added).

In contrast, the cited prior art does not render the memory cell of claim 38 obvious. Specifically, as amply demonstrated above, DiMaria, Lee, and Rinerson fail to teach or suggest, collectively or separately, "said storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the silicon-rich insulator with the first conductive layer." (Claim 38).

Again, under the analysis required by *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966), to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by DiMaria, Lee, and Rinerson, did not include the claimed subject matter, particularly "said storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the silicon-rich insulator with the first conductive layer." (Claim 38).

The differences between the cited prior art and the indicated claims are significant because the low-resistance filament provides an improved way of writing data into a storage element such as a tunnel-junction oxide or a state-change layer. (Applicant's Specification, p. 8, lines 26-28). Thus, the claimed subject matter provides features and advantages not known or available in the cited prior art. Consequently, the cited prior art will not support a rejection of claim 38 under 35 U.S.C. § 103 and *Graham*. For at least these reasons, the rejection of claim 38 and its dependent claims based on DiMaria, Lee, and Rinerson, or alternatively based on Lee and DiMaria, should be reconsidered and withdrawn.

Claim 47:

Claim 47 recites:

> A multilayer memory made by a method comprising:
> a) providing a substrate,
> b) depositing and patterning a first conductive layer over the substrate,
> c) forming a storage layer over the patterned first conductive layer, *said storage layer comprising a low-resistance filament disposed therein*,
> d) forming and patterning a first interlayer dielectric over the storage layer,
> e) forming an opening through the first interlayer dielectric and extending to the storage layer,
> f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, *said middle electrode being electrically coupled to said first conductive layer through said low-resistance filament of said storage layer,*
> g) forming a layer of silicon-rich insulator over at least the first interlayer dielectric, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,
> h) forming a tunnel-junction layer over the layer of silicon-rich insulator,
> i) forming and patterning a second conductive layer over the tunnel-junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,
> j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and
l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

In contrast, the cited prior art does not render the multilayer memory of claim 47 obvious. Specifically, as amply demonstrated above, DiMaria, Lee, and Rinerson fail to teach or suggest, collectively or separately, "said storage layer comprising a low-resistance filament disposed therein" or "said middle electrode being electrically coupled to said first conductive layer through said low-resistance filament of said storage layer." (Claim 47).

Again, under the analysis required by *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966), to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by DiMaria, Lee, and Rinerson, did not include the claimed subject matter, particularly "said storage layer comprising a low-resistance filament disposed therein" or "said middle electrode being electrically coupled to said first conductive layer through said low-resistance filament of said storage layer." (Claim 47).

The differences between the cited prior art and the indicated claims are significant because the low-resistance filament provides an improved way of writing data into a storage element such as a tunnel-junction oxide or a state-change layer. (Applicant's Specification, p. 8, lines 26-28). Thus, the claimed subject matter provides features and advantages not known or available in the cited prior art. Consequently, the cited prior art will not support a rejection of claim 47 under 35 U.S.C. § 103 and *Graham*. For at least these reasons, the rejection of

claim 47 and its dependent claims based on DiMaria, Lee, and Rinerson, or alternatively based on Lee and DiMaria, should be reconsidered and withdrawn.

Claim 55:

Claim 55 recites:

A multilayer memory made by a method comprising:

a) providing a substrate,

b) depositing and patterning a first conductive layer over the substrate,

c) forming a tunnel-junction layer over the first conductive layer,

d) forming a layer of silicon-rich insulator over the tunnel-junction layer,

e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,

f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator,

h) forming a storage-element layer over the patterned first interlayer dielectric, *said storage-element layer comprising a low-resistance filament disposed therein,*

i) forming and patterning a second conductive layer over the storage-element layer, the patterned second conductive layer being disposed to overlay vertically at least a portion of the middle electrode, such that a portion of the second conductive layer is aligned with some portion of the middle electrode, *wherein the low-resistance filament of the storage element electrically interconnects the layer of silicon-rich insulator with the middle electrode*, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

In contrast, the cited prior art does not render the multilayer memory of claim 55 obvious. Specifically, as amply demonstrated above, DiMaria, Lee, and Rinerson fail to teach or suggest, collectively or separately, "said storage layer comprising a low-resistance filament

disposed therein" or "wherein the low-resistance filament of the storage element electrically interconnects the layer of silicon-rich insulator with the middle electrode." (Claim 55).

Again, under the analysis required by *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17-18 (1966), to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by DiMaria, Lee, and Rinerson, did not include the claimed subject matter, particularly "said storage layer comprising a low-resistance filament disposed therein" or "wherein the low-resistance filament of the storage element electrically interconnects the layer of silicon-rich insulator with the middle electrode." (Claim 55).

The differences between the cited prior art and the indicated claims are significant because the low-resistance filament provides an improved way of writing data into a storage element such as a tunnel-junction oxide or a state-change layer. (Applicant's Specification, p. 8, lines 26-28). Thus, the claimed subject matter provides features and advantages not known or available in the cited prior art. Consequently, the cited prior art will not support a rejection of claim 55 under 35 U.S.C. § 103 and *Graham*. For at least these reasons, the rejection of claim 55 and its dependent claims based on DiMaria, Lee, and Rinerson, or alternatively based on Lee and DiMaria, should be reconsidered and withdrawn.

Claims 5-6 and 8-10:

The rejection of dependent claims 5-6 and 8-10 should be withdrawn for at least the same reasons given above in favor of the patentability of independent claim 1. Additionally, the Examiner has taken Official Notice with respect to these claims that:

> [I]t would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element of each memory cell comprises [sic] a tunnel junction layer thickness of about 3-5 nanometers, and the storage element of each memory cell comprises an anti-fuse, a fuse, a tunnel junction, a state-change layer and a chalcogenide, in prior art's device [sic] in order to use known memory control and storage elements.

(Action, p. 8).

In response, Applicant expressly does not acquiesce to the taking of Official Notice, and respectfully requests that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

2. Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49, and 55-59 were rejected under 35 U.S.C. § 103(a) as being obvious over Lee in view of U.S. Patent No. 7,012,297 to Bhattacharyya ("Bhattacharyya"), U.S. Patent No. 4,717,943 to Wolf et al. ("Wolf"), and U.S. Patent No. 4,870,470 to Bass Jr. et al. ("Bass"). These same claims were rejected alternatively under § 103(a) as being obvious over Bass in view of Lee and Rinerson. For at least the following reasons, these rejections are respectfully traversed.

Claim 1:

Claim 1 recites:

> A memory array comprising:
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points,

and

b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, *each storage element comprising a low-resistance filament disposed therein,* each control element including a tunnel junction and a silicon-rich insulator, *wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor*, and *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*

(Emphasis added).

The Examiner has also failed to meet the Office's burden to establish a *prima facie* case of obviousness against the claimed subject matter to sustain the present rejection.

Applicant notes that in the two terminal memory cell taught in Applicant's specification, a memory cell "is selected" by applying a voltage difference between the two terminals of the memory cell. (*See e.g.,* Applicant's specification, pp. 13-14 and Figs. 14-15). During a read operation, a read voltage is applied to the terminals and an amount of current flowing between the terminals is measured with a sense amplifier. (*Id.*). During a write operation, the cell is selected by applying a write voltage differential to the terminals that is different from the read voltage to change a storage state of the storage element in the memory cell. (*See Id.* at pp. 6, 13-14 and Figs. 14-15).

In light of the above, Applicant's specification defines memory cell selection as necessarily encompassing memory cell selection during both read and write operations. Because the meaning of words used in the claims is determined by the meaning given to those words in the specification, a prior art memory cell must be evaluated during both read and write operations to determine the behavior of the memory cell when it "is selected." (Claim 1; s*ee Markman v. Westview Instruments*, 116 S. Ct. 1384 (1996); *McGill, Inc. v. John Zink Co.*, 736 F.2d 666, 674 (Fed. Cir. 1984); *ZMI Corp. v. Cardiac Resuscitator Corp.* 884 F.2d 1576, 1580, 6 U.S.P.Q.2d 1557, 1560-61 (Fed. Cir. 1988) ("words must be used in the same

way in both the claims and the specification.")). Furthermore, because Applicant's specification defines a "control element" as "for controlling **write and read** operations" in a memory cell, any assertion that the prior art teaches a control element as recited in claim 1 must be evaluated in light of whether the cited prior art elements are configured to control **both** write and read operations. (Applicant's specification, p.2)

Turning now to the cited prior art, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest a memory cell having "a control element" that includes "a tunnel junction and a silicon-rich insulator, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected." (Claim 1). The final Office Action concedes the shortcomings of Lee in this regard. Specifically, the final Office Action states that Lee does "not teach a control element including a tunnel junction and a silicon-rich oxide insulator, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected." (Action, p. 11).

Consequently, the Action cites to Bhattacharyya. According to the final Office Action, Bhattacharyya teaches "a control element including a tunnel junction and a silicon-rich oxide insulator 1154, wherein the silicon rich insulator injects current into the tunnel junction when the memory cell is selected." (Action, p. 11). Applicant respectfully disagrees.

Bhattacharyya teaches a field-effect transistor based memory cell that has three terminals—a drain, a source and a gate stack. (*See, e.g.*, Bhattacharyya at Figs. 6-14 and col. 7, lines 16-38). The gate stack includes at least "a control gate," a first "injector layer," a "charge blocking layer," a "tunnel layer," and a second "injector layer." (*Id.* at Fig. 11). The injector layers may include silicon-rich nitride (SRN) material. (*See, e.g., Id.* at col. 12, lines 11-18). A digital "1" value can be written to the memory cell of Bhattacharyya by applying a

"programming voltage" to the control gate of the gate stack, thereby injecting a sufficient amount of charge into the tunnel layer of the gate stack such that a voltage difference between the gate of the field-effect transistor and the source of the field-effect transistor is maintained at a level greater than a device-characteristic threshold voltage, effectively creating a short circuit between the drain and the source of the transistor. (*See, e.g., Id.* at col. 8, lines 9-22; Fig. 9). Similarly, a "0" is stored in the memory cell when gate stack does not store a sufficient amount of charge to create a voltage difference between the gate and the source of the transistor that is greater than the threshold voltage, thereby effectively creating an open circuit between the drain and the source of the transistor. (*Id.*).

Bhattacharyya does not explicitly describe how data is read from the memory cell it teaches. However, the processing of reading data from the three-terminal FET-based memory cells to which Bhattacharyya is directed are well-known in the art and readily apparent from the inherent physical characteristics of the cells. To read a digital value stored by the memory cell of Bhattacharyya, the memory cell must first be selected by applying a voltage difference between the drain and the source of the FET transistor. Then current flow between the drain and the source is measured, for example with one or more sense amplifiers. If the measured current flow is greater than a predetermined amount, a digital "1" is read from the memory cell. Otherwise, a digital "0" is read. No voltage can be applied to the gate stack of a FET-based memory cell during a read cycle due to the likely corruption of the data being read from the memory cell.

Applicant wishes to point out that the gate stack taught by Bhattacharyya is only used to control write operations of its associated memory cell. Read operations in the memory cell are performed independently without applying any kind of change in voltage to the gate stack or measuring a voltage or current at the gate stack. Therefore, because the gate stack of

Bhattacharyya does not "[control] write and read operations" of its associated memory cell, the gate stack **cannot** read on the control element recited in claim 1. (Applicant's specification, p.2) Bhattacharyya utterly fails to teach or suggest such a control element anywhere.

Applicant further notes that even if the gate stack taught by Bhattacharyya could be considered a "control element" as defined in Applicant's specification, due to the inherent requirement that voltage be applied to the gate stack for one of the injector layers in the gate stack to inject current into the tunnel layer of the gate stack, charge cannot be injected into the tunnel layer of the gate stack when the memory cell is selected for a read operation. Therefore, Bhattacharyya does not teach or suggest the injection of charge into the tunnel layer of the gate stack when the memory cell is selected for a read operation under any circumstances. Because of Bhattacharyya's failure to teach or suggest this subject matter, Bhattacharyya **cannot** teach or suggest a memory cell having a "control element including a tunnel junction and a silicon-rich insulator, *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*" (Claim 1) (emphasis added).

Turning now to Wolf, the final Office Action alleges that Wolf teaches "in Figure 2 and related text a control element including a tunnel junction 16 and a silicon-rich oxide insulator 20, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected." (Action, pp. 11-12). Applicant respectfully disagrees. Like Bhattacharyya, Wolf teaches a three-terminal FET-based memory cell having a gate stack. The gate stack includes a layer 16 of silicon dioxide that may function as a tunnel junction and a layer 20 of silicon-rich oxide disposed between the layer 16 of silicon dioxide and an upper electrode 12. (Wolf, col. 2, lines 36-45 and 55-65). However, like Bhattacharyya, the three-terminal memory cell taught by Wolf follows the well-known conventions of three-

terminal FET-based memory cells in the art, in that the memory cell is selected for a read operation by applying a voltage difference between a drain and a source in the FET, during which time voltage may not be applied to the gate stack. (*See* Wolf, col. 2, lines 15-20).

Therefore, like its counterpart in Bhattacharyya, the gate stack taught by Wolf is only used to control write operations of its associated memory cell. Read operations in the memory cell are performed independently without applying any kind of change in voltage to the gate stack or measuring a voltage or current at the gate stack. Therefore, because the gate stack of Wolf does not "[control] write and read operations" of its associated memory cell, the gate stack **cannot** read on the control element recited in claim 1. (Applicant's specification, p.2) Wolf utterly fails to teach or suggest such a control element anywhere.

Furthermore, because voltage is not applied to the gate stack of the memory cell taught by Wolf when the memory cell is selected for a read operation, the layer 20 of silicon-rich oxide in the gate stack *cannot* inject current into the tunnel junction 16 of the gate stack when the memory cell is selected for a read operation. Moreover, Wolf does not teach or suggest anywhere that the layer 20 of silicon-rich oxide in the gate stack injects current into the tunnel junction 16 when the memory cell is selected for a read operation. Accordingly, Wolf **cannot** teach or suggest a memory cell having a "control element including a tunnel junction and a silicon-rich insulator, *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*" (Claim 1) (emphasis added).

Turning now to Bass, the final Office Action alleges that Bass "teach[es] in Figure 6 and related text a control element including a tunnel junction and a silicon-rich insulator 35, wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected." (Action, p. 12). Applicant again respectfully disagrees.

Applicant notes that Bass, like Bhattacharyya and Wolf, is directed to a three-terminal FET-based memory cell having a gate stack configured to store charge according to the digital value written to the memory cell. The gate stack of Bass includes a silicon-rich silicon nitride film 30 deposited on top of a silicon oxide layer 20 and having a barrier layer 25 formed on the silicon-rich silicon nitride film, and a charge injection structure 35 deposited on the barrier layer 25. (Bass, col. 7, lines 40-57; col. 8, lines 3-4; Fig. 6).

The gate stack taught by Bass, just like its counterparts in Bhattacharyya and Wolf, is only used to control write operations of its associated memory cell. Read operations in the memory cell are performed independently without applying any kind of change in voltage to the gate stack or measuring a voltage or current at the gate stack. Therefore, because the gate stack of Bass does not "[control] write and read operations" of its associated memory cell, the gate stack **cannot** read on the control element recited in claim 1. (Applicant's specification, p. 2) Bass utterly fails to teach or suggest such a control element anywhere.

Moreover, Bass does not teach anywhere that the silicon-rich silicon nitride film 30 injects current into either the silicon oxide layer 20 or the barrier layer 25 when the memory cell is selected for a read process. Further, such current injection could not occur while maintaining reliable functionality of the memory cell of Bass for the reasons given above with respect to the analogous three-terminal FET-based memory cells taught by Bhattacharyya and Wolf. Accordingly, Bass **cannot** teach or suggest a memory cell having a "control element including a tunnel junction and a silicon-rich insulator, *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*" (Claim 1, emphasis added).

Furthermore, Applicant notes that none of Lee, Bhattacharyya, Wolf, and Bass teaches or suggests the additional subject matter recited in the amendment of claim 1. Specifically,

Lee, Bhattacharyya, Wolf, and Bass all fail to teach or suggest "each storage element comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 1).

Applicant notes that the present rejection relies on an assertion of obviousness based on the combination of prior art elements according to known methods to yield predictable results. According to the M.P.E.P., "[t]o reject a claim based on this rationale, Office personnel must resolve the . . . factual inquiries" of *Graham*, 383 U.S. at 17-18. M.P.E.P. § 2143.

Under the analysis required by *Graham*, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. *Graham*, 383 U.S. at 17-18. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. While it is true that attacking references individually is not sufficient to demonstrate nonobviousness, *Keller*, 642 F.2d at 208, the scope and content of the prior art as a whole may only be determined by a methodical examination of each prior art reference to determine what each reference teaches and does not teach. If such an examination reveals that *each* cited prior art reference fails to teach or suggest a particular claimed element, it follows that the scope and content of the cited prior art does not include that element.

Applying the *Graham* analysis to the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a control element with a tunnel junction, a silicon-rich insulator that injects current into the tunnel junction when the memory

cell is selected, or "each storage element comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 1). This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 1 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should be reconsidered and withdrawn.

Claim 16:

Claim 16 recites:

> A memory array comprising:
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, *each means for storing data comprising a low-resistance filament disposed therein, each means for controlling including a tunnel junction and a silicon-rich insulator, wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor*, and *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a "silicon-rich insulator [that] injects

current into the tunnel junction when the memory cell is selected" or "each means for storing data comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 16).

Again, under the analysis required by *Graham*, 383 U.S. at 17-18, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising means for controlling that comprises a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected or "each means for storing data comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 16). This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 16 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should be reconsidered and withdrawn in view of 35 U.S.C. § 103 and *Graham*.

Claim 26:

Claim 26 recites:

> A memory cell made by a method comprising:
> a) providing a substrate,
> b) depositing and patterning a first conductive layer over the substrate,
> c) forming a storage layer over the patterned first conductive layer, *the storage layer comprising a low-resistance filament disposed therein*,
> d) forming a layer of silicon-rich insulator over the storage layer,
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and
> f) forming and patterning a second conductive layer over the tunnel-junction layer, whereby a memory-cell stack is formed, the stack having a storage layer, a silicon-rich insulator, and a tunnel-junction layer in series relationship between the first and second conductive layers, such that the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *wherein the low-resistance filament of the storage layer electrically interconnects the layer of silicon-rich insulator with the first conductive layer*, and *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected" or "the storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the layer of silicon-rich insulator with the first conductive layer." (Claim 26).

Again, under the analysis required by *Graham*, 383 U.S. at 17-18, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. 398 at 407 (2007). In the present case, the scope and content of

the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected and "the storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the layer of silicon-rich insulator with the first conductive layer." (Claim 26). This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 26 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should be reconsidered and withdrawn in view of 35 U.S.C. § 103 and *Graham*.

Claim 38:

Claim 38 recites:

> A memory cell made by a method comprising:
> a) providing a substrate,
> b) depositing and patterning a first conductive layer over the substrate,
> c) forming a storage layer over the patterned first conductive layer, *said storage layer comprising a low-resistance filament disposed therein*,
> d) forming a layer of silicon-rich insulator over the storage layer,
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator,
> f) forming and patterning a second conductive layer over the tunnel-junction layer,
> g) forming and patterning an interlayer dielectric over the storage layer,
> h) forming an opening through the interlayer dielectric and extending to the storage layer, and
> i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of

> the memory cell, *and wherein the low-resistance filament of the storage layer electrically interconnects the silicon-rich insulator with the first conductive layer*, and *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, a "storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the silicon-rich insulator with the first conductive layer," and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected." (Claim 38).

Again, under the analysis required by *Graham*, 383 U.S. at 17-18, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator, a "storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the silicon-rich insulator with the first conductive layer," and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected." (Claim 38). This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 38 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should be reconsidered and withdrawn in view of 35 U.S.C. § 103 and *Graham*.

Claim 47:

Claim 47 recites:

> A multilayer memory made by a method comprising:
> a) providing a substrate,
> b) depositing and patterning a first conductive layer over the substrate,
> c) forming a storage layer over the patterned first conductive layer, *said storage layer comprising a low-resistance filament disposed therein*,
> d) forming and patterning a first interlayer dielectric over the storage layer,
> e) forming an opening through the first interlayer dielectric and extending to the storage layer,
> f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, *said middle electrode being electrically coupled to said first conductive layer through said low-resistance filament of said storage layer,*
> g) forming a layer of silicon-rich insulator over at least the first interlayer dielectric, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,
> h) forming a tunnel-junction layer over the layer of silicon-rich insulator,
> i) forming and patterning a second conductive layer over the tunnel-junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,
> j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,
> k) forming vias as required through the second interlayer dielectric, and
> l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected," "said storage layer comprising a low-resistance filament disposed therein," or "said middle electrode being electrically coupled to said first conductive layer through said low-resistance filament of said storage layer." (Claim 47).

Again, under the analysis required by *Graham*, 383 U.S. at 17-18, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected," "said storage layer comprising a low-resistance filament disposed therein," or "said middle electrode being electrically coupled to said first conductive layer through said low-resistance filament of said storage layer." (Claim 47).

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 47

and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should be reconsidered and withdrawn in view of 35 U.S.C. § 103 and *Graham*.

Claim 55:

Claim 55 recites:

A multilayer memory made by a method comprising:
a) providing a substrate,
b) depositing and patterning a first conductive layer over the substrate,
c) forming a tunnel-junction layer over the first conductive layer,
d) forming a layer of silicon-rich insulator over the tunnel-junction layer,
e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,
f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,
g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator,
h) forming a storage-element layer over the patterned first interlayer dielectric, *said storage-element layer comprising a low-resistance filament disposed therein,*
i) forming and patterning a second conductive layer over the storage-element layer, the patterned second conductive layer being disposed to overlay vertically at least a portion of the middle electrode, such that a portion of the second conductive layer is aligned with some portion of the middle electrode, *wherein the low-resistance filament of the storage element electrically interconnects the layer of silicon-rich insulator with the middle electrode*, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,
j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,
k) forming vias as required through the second interlayer dielectric, and
l) repeating steps b) through k) until a desired number of memory array layers have been formed.
(Emphasis added).

As demonstrated above in connection with claim 1, Lee, Bhattacharyya, Wolf, and Bass utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected," "said storage layer

comprising a low-resistance filament disposed therein" or "wherein the low-resistance filament of the storage element electrically interconnects the layer of silicon-rich insulator with the middle electrode." (Claim 55).

Again, under the analysis required by *Graham*, 383 U.S. at 17-18, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator, a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected," "said storage layer comprising a low-resistance filament disposed therein" or "wherein the low-resistance filament of the storage element electrically interconnects the layer of silicon-rich insulator with the middle electrode." (Claim 55). This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 55 and its dependent claims based on Lee, Bhattacharyya, Wolf, and Bass should be reconsidered and withdrawn in view of 35 U.S.C. § 103 and *Graham*.

Claims 5-6 and 8-10:

The rejection of dependent claims 5-6 and 8-10 should be withdrawn for at least the same reasons given above in favor of the patentability of independent claim 1. Additionally, the Examiner has taken Official Notice with respect to these claims that:

> [I]t would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element of each memory cell comprises [sic] a tunnel junction layer thickness of about 3-5 nanometers, and the storage element of each memory cell comprises an anti-fuse, a fuse, a tunnel junction, a state-change layer and a chalcogenide, in prior art's device [sic] in order to use known memory control and storage elements.

(Action, p. 14).

In response, Applicant expressly does not acquiesce to the taking of Official Notice, and respectfully requests that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

3. Claims 1, 3-6, 8-11, 16, 26-33, 38-41, 47-49, and 55-59 were alternatively rejected under 35 U.S.C. § 103(a) as obvious over Bass, Lee, and Rinerson. For at least the following reasons, this rejection is respectfully traversed.

Claim 1:

Claim 1:

Claim 1 recites:

> A memory array comprising:
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals and having a storage element and a control element coupled in series between a row conductor and a column conductor, *each storage element comprising a low-resistance filament disposed therein,* each control element including a tunnel junction and a silicon-rich insulator, *wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the*

row conductor and the column conductor, and wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.

(Emphasis added).

Again,"[t]he examiner bears the initial burden . . . of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). A *prima facie* case of obviousness made under 35 U.S.C. § 103(a) requires a showing that all of the subject matter in the claim at issue would be obvious to one having ordinary skill in the art based on the teachings of the cited prior art. *See* M.P.E.P. § 2143. The recent Office Action does not make a *prima facie* case of obviousness against claim 1 because it fails to provide sufficient evidence that the cited prior art would render all of the subject matter of claim 1 obvious to one having ordinary skill in the art at the time of the invention. *Id.*

In contrast, as amply demonstrated above, Bass, Lee, and Rinerson do not render claim 1 obvious. Specifically, as amply demonstrated above, Bass, Lee, and Rinerson do not teach or suggest various elements recited in claim 1, including a control element with a tunnel junction, a silicon-rich insulator that injects current into the tunnel junction when the memory cell is selected, or "each storage element comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 1).

Under the analysis required by *Graham*, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. *Graham*, 383 U.S. at 17-18. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103.

KSR, 550 U.S. at 407. While it is true that attacking references individually is not sufficient to demonstrate nonobviousness, *Keller*, 642 F.2d at 208, the scope and content of the prior art as a whole may only be determined by a methodical examination of each prior art reference to determine what each reference teaches and does not teach. If such an examination reveals that *each* cited prior art reference fails to teach or suggest a particular claimed element, it follows that the scope and content of the cited prior art does not include that element.

Applying the *Graham* analysis to the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a control element with a tunnel junction, a silicon-rich insulator that injects current into the tunnel junction when the memory cell is selected, or "each storage element comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 1). This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 1 and its dependent claims based on Bass, Lee, and Rinerson should be reconsidered and withdrawn.

Claim 16:

Claim 16 recites:

> A memory array comprising:
> a) a multiplicity of row conductors and a multiplicity of column conductors, the row conductors and column conductors being arranged to cross at cross-points, and
> b) a memory cell disposed at each cross-point, each memory cell having exactly two terminals, each memory cell comprising means for storing data and means for controlling the means for storing data, the means for storing data and means for controlling being coupled in series between a row conductor and a column conductor, *each means for storing data comprising a low-resistance filament disposed therein, each means for controlling including a tunnel junction and a silicon-rich insulator, wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor*, and *wherein the silicon-rich insulator injects current into the tunnel junction when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claim 1, Bass, Lee, and Rinerson utterly fail to teach or suggest this subject matter of a "silicon-rich insulator [that] injects current into the tunnel junction when the memory cell is selected" or "each means for storing data comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 16).

Again, under the analysis required by *Graham*, 383 U.S. at 17-18, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by Bass, Lee, and Rinerson, did not include the claimed subject matter, particularly the claimed memory cell comprising means for controlling that comprises a

silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected or "each means for storing data comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage element electrically interconnects the silicon-rich insulator with one of the row conductor and the column conductor." (Claim 16). This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 16 and its dependent claims based on Bass, Lee, and Rinerson should be reconsidered and withdrawn in view of 35 U.S.C. § 103 and *Graham*.

Claim 26:

Claim 26 recites:

> A memory cell made by a method comprising:
> a) providing a substrate,
> b) depositing and patterning a first conductive layer over the substrate,
> c) forming a storage layer over the patterned first conductive layer, *the storage layer comprising a low-resistance filament disposed therein*,
> d) forming a layer of silicon-rich insulator over the storage layer,
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator, and
> f) forming and patterning a second conductive layer over the tunnel-junction layer, whereby a memory-cell stack is formed, the stack having a storage layer, a silicon-rich insulator, and a tunnel-junction layer in series relationship between the first and second conductive layers, such that the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *wherein the low-resistance filament of the storage layer electrically interconnects the layer of silicon-rich insulator with the first conductive layer*, and *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claim 1, Bass, Lee, and Rinerson utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected" or "the storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the layer of silicon-rich insulator with the first conductive layer." (Claim 26).

Again, under the analysis required by *Graham*, 383 U.S. at 17-18, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. 398 at 407 (2007). In the present case, the scope and content of the prior art, as evidenced by Lee, Bhattacharyya, Wolf, and Bass, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator that injects current into a tunnel junction when the memory cell is selected and "the storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the layer of silicon-rich insulator with the first conductive layer." (Claim 26). This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 26

and its dependent claims based on Bass, Lee, and Rinerson should be reconsidered and withdrawn in view of 35 U.S.C. § 103 and *Graham*.

Claim 38:

Claim 38 recites:

> A memory cell made by a method comprising:
> a) providing a substrate,
> b) depositing and patterning a first conductive layer over the substrate,
> c) forming a storage layer over the patterned first conductive layer, *said storage layer comprising a low-resistance filament disposed therein*,
> d) forming a layer of silicon-rich insulator over the storage layer,
> e) forming a tunnel-junction layer over the layer of silicon-rich insulator,
> f) forming and patterning a second conductive layer over the tunnel-junction layer,
> g) forming and patterning an interlayer dielectric over the storage layer,
> h) forming an opening through the interlayer dielectric and extending to the storage layer, and
> i) filling the opening through the interlayer dielectric with conductive material to form a middle electrode contiguous with the storage layer, wherein the first and second conductive layers are adapted to provide exactly two terminals for control of the memory cell, *and wherein the low-resistance filament of the storage layer electrically interconnects the silicon-rich insulator with the first conductive layer*, and *wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected.*

(Emphasis added).

As demonstrated above in connection with claim 1, Bass, Lee, and Rinerson utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, a "storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the silicon-rich insulator with the first conductive layer," and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected." (Claim 38).

Again, under the analysis required by *Graham*, 383 U.S. at 17-18, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by Bass, Lee, and Rinerson, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator, a "storage layer comprising a low-resistance filament disposed therein . . . wherein the low-resistance filament of the storage layer electrically interconnects the silicon-rich insulator with the first conductive layer," and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected." (Claim 38). This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 38 and its dependent claims based on Bass, Lee, and Rinerson should be reconsidered and withdrawn in view of 35 U.S.C. § 103 and *Graham*.

Claim 47:

Claim 47 recites:

> A multilayer memory made by a method comprising:
> a) providing a substrate,
> b) depositing and patterning a first conductive layer over the substrate,

c) forming a storage layer over the patterned first conductive layer, *said storage layer comprising a low-resistance filament disposed therein*,

d) forming and patterning a first interlayer dielectric over the storage layer,

e) forming an opening through the first interlayer dielectric and extending to the storage layer,

f) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, *said middle electrode being electrically coupled to said first conductive layer through said low-resistance filament of said storage layer,*

g) forming a layer of silicon-rich insulator over at least the first interlayer dielectric, at least a portion of the silicon-rich insulator being disposed contiguous with the middle electrode,

h) forming a tunnel-junction layer over the layer of silicon-rich insulator,

i) forming and patterning a second conductive layer over the tunnel-junction layer and disposed to overlay vertically at least a portion of the middle electrode, whereby a portion of the second conductive layer is aligned with some portion of the middle electrode, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

As demonstrated above in connection with claim 1, Bass, Lee, and Rinerson utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected," "said storage layer comprising a low-resistance filament disposed therein," or "said middle electrode being electrically coupled to said first conductive layer through said low-resistance filament of said storage layer." (Claim 47).

Again, under the analysis required by *Graham*, 383 U.S. at 17-18, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim

at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art, as evidenced by Bass, Lee, and Rinerson, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator, and a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected," "said storage layer comprising a low-resistance filament disposed therein," or "said middle electrode being electrically coupled to said first conductive layer through said low-resistance filament of said storage layer." (Claim 47).

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 47 and its dependent claims based on Bass, Lee, and Rinerson should be reconsidered and withdrawn in view of 35 U.S.C. § 103 and *Graham*.

Claim 55:

Claim 55 recites:

A multilayer memory made by a method comprising:
a) providing a substrate,
b) depositing and patterning a first conductive layer over the substrate,
c) forming a tunnel-junction layer over the first conductive layer,
d) forming a layer of silicon-rich insulator over the tunnel-junction layer,
e) forming and patterning a first interlayer dielectric over the layer of silicon-rich insulator,
f) forming an opening through the first interlayer dielectric and extending to the layer of silicon-rich insulator,

g) filling the opening through the first interlayer dielectric with conductive material to form a middle electrode, at least a portion of the middle electrode being disposed contiguous with the silicon-rich insulator,

h) forming a storage-element layer over the patterned first interlayer dielectric, *said storage-element layer comprising a low-resistance filament disposed therein,*

i) forming and patterning a second conductive layer over the storage-element layer, the patterned second conductive layer being disposed to overlay vertically at least a portion of the middle electrode, such that a portion of the second conductive layer is aligned with some portion of the middle electrode, *wherein the low-resistance filament of the storage element electrically interconnects the layer of silicon-rich insulator with the middle electrode*, and wherein the first and second conductive layers are adapted to provide exactly two terminals for control of a memory cell, and wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected,

j) forming and patterning a second interlayer dielectric over the patterned second conductive layer, whereby a substrate is formed for subsequent layers,

k) forming vias as required through the second interlayer dielectric, and

l) repeating steps b) through k) until a desired number of memory array layers have been formed.

(Emphasis added).

As demonstrated above in connection with claim 1, Bass, Lee, and Rinerson utterly fail to teach or suggest this subject matter of a memory cell that comprises a silicon-rich insulator, a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected," "said storage layer comprising a low-resistance filament disposed therein" or "wherein the low-resistance filament of the storage element electrically interconnects the layer of silicon-rich insulator with the middle electrode." (Claim 55).

Again, under the analysis required by *Graham*, 383 U.S. at 17-18, to support a rejection under 35 U.S.C. § 103, the scope and content of the prior art must first be determined, followed by an assessment of the differences between the prior art and the claim at issue in view of the ordinary skill in the art. The Supreme Court has recently reaffirmed that the *Graham* factors "continue to define the inquiry that controls" obviousness rejections under § 103. *KSR*, 550 U.S. at 407. In the present case, the scope and content of the prior art,

as evidenced by Bass, Lee, and Rinerson, did not include the claimed subject matter, particularly the claimed memory cell comprising a silicon-rich insulator, a tunnel-junction layer "wherein the silicon-rich insulator injects current into the tunnel-junction layer when the memory cell is selected," "said storage layer comprising a low-resistance filament disposed therein" or "wherein the low-resistance filament of the storage element electrically interconnects the layer of silicon-rich insulator with the middle electrode." (Claim 55). This subject matter is entirely outside the scope and content of the cited prior art.

These differences between the cited prior art and the claimed subject matter are significant because the claimed subject matter enhances the operation of two-terminal non-FET memory cells. Therefore, the claimed subject matter provides features and advantages not known or available in the prior art. For at least these reasons, the rejection of claim 55 and its dependent claims based on Bass, Lee, and Rinerson should be reconsidered and withdrawn in view of 35 U.S.C. § 103 and *Graham*.

Claims 5-6 and 8-10:

The rejection of dependent claims 5-6 and 8-10 should be withdrawn for at least the same reasons given above in favor of the patentability of independent claim 1. Additionally, the Examiner has taken Official Notice with respect to these claims that:

> [I]t would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a control element of each memory cell comprises [sic] a tunnel junction layer thickness of about 3-5 nanometers, and the storage element of each memory cell comprises an anti-fuse, a fuse, a tunnel junction, a state-change layer and a chalcogenide, in prior art's device [sic] in order to use known memory control and storage elements.

(Action, p. 14).

In response, Applicant expressly does not acquiesce to the taking of Official Notice, and respectfully requests that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

Conclusion:

In view of the preceding arguments, all claims are believed to be in condition for allowance over the prior art of record. Therefore, this response is believed to be a complete response to the Office Action. However, Applicant reserves the right to set forth further arguments in future papers supporting the patentability of any of the claims, including the separate patentability of the dependent claims not explicitly addressed herein. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed.

The absence of a reply to a specific rejection, issue or comment in the Office Action does not signify agreement with or concession of that rejection, issue or comment. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment. Further, for any instances in which the Examiner took Official Notice in the Office Action, Applicants expressly do not acquiesce to the taking of Official Notice, and respectfully request that the Examiner provide an affidavit to support the Official Notice taken in the next Office Action, as required by 37 CFR 1.104(d)(2) and MPEP § 2144.03.

If the Examiner has any comments or suggestions which could place this application in better form, the Examiner is requested to telephone the undersigned attorney at the number listed below.

Respectfully submitted,

DATE: 7 April 2010

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